error-containing code in the error correcting code word; and

said odd-numbered error correction sub means is an odd-numbered error correction sub means with mid-term results for, in the third-time or later odd-numbered error correction, making said bus control means start a concurrent data transfer not at the head but at the code word of each sector from which an error-containing code has been detected, based on the information designated by said sector-basis non-error code word range designating sub means; for making said syndrome calculating means start syndrome calculation at the code word; and for making said error detecting means start error detection at a code word somewhere in the middle of the sector by using contents stored in said sector-basis storing means as an initial value.

11. The error correction device of claim 7 or 8 further comprising a sector-group-basis storing means for storing mid-term results, on a sector-group-by-sector-group-basis, in code word units, of each code word from which no error has been detected in the error detecting process done by said error detecting means until said syndrome calculating means detects an error-containing code, wherein

said non-error range designating sub means is a sector-group-basis non-error code word range designating sub means for designating, on a sector-group-by-sector-group-basis, in code word units, a range from which an error-containing code has not been detected in the odd-numbered error correction or the subsequent even-numbered error correction, based on said information that designates the code word including the error-containing

code and on said information that designates the position of the error-containing code in the error correcting code word; and

said odd-numbered error correction sub means is an odd-numbered error correction sub means with mid-term results for, in the third-time or later odd-numbered error correction, making said bus control means start a concurrent data transfer not at the head but at the code word of each sector group from which an error-containing code has been detected, based on the information designated by said sector-group-basis non-error code word range designating sub means; for making said syndrome calculating means start syndrome calculation at the code word; and for making said error detecting means start error detection at a code word somewhere in the middle of the sector by using contents stored in said sector-group-basis storing means as an initial value.

12. The error correction device of claim 1, 2, 5, 6, 7, or 8, wherein error correction is performed in parallel for data in a plurality of ECC blocks each having a structure where a plurality of error correcting code words each comprising a data unit and a parity unit are arranged in vertical direction and horizontal direction so as to repeat error correction a plurality of number of times, and where predetermined data composed of a predetermined number of code words in the vertical direction or the horizontal direction (data in the horizontal direction are referred to as sector) as a unit are subjected to the error correction, wherein

said buffer memory is a plural-ECC-block-division buffer memory corresponding to a plurality of ECC blocks to be processed in parallel;

said storing means for storing mid-term results of an error detecting process generated by said error detecting means is an ECC-block-division storing means for storing said plurality of ECC blocks on a block-by-block basis;

said system control means comprises:

a means-basis ECC block pipeline processing notification sub means for transmitting ECC blocks which have been subjected to error correction downstream; for storing ECC blocks to be processed next to said plural-ECC-block-division buffer memory; and for making the storage known to said bus control means, said syndrome calculating means, said error detecting means, and said error correcting means;

a means-basis ECC block recognition sub means for recognizing a data transfer from said bus control means to said syndrome calculating means, to said error detecting means, and to said error correcting means for error detection and error correction; for recognizing the error correction done by said error correcting means; for recognizing writing of error-corrected data to said plural-ECC-block-division buffer memory done by said bus control means; for recognizing an ECC block in process when said error detecting means stores mid-term results to said plural-ECC-block-division storing means, and for selecting ECC blocks to be processed; and

an ECC block notification sub means in sub means-basis pipeline processing for notifying said first error detecting sub means, said even-numbered error correction sub means, said odd-numbered error correction sub means, said number-of-times control sub means, and said